IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND claims 1 and 3-7 in accordance with the following:

1. (CURRENTLY AMENDED) A timing extraction circuit which uses ~~a PLL circuit~~ a Phase Locked Loop (PLL) circuit containing a phase comparator circuit ~~for~~ performing a phase comparison between a data signal of bit rate B (bits/s) and a clock signal of B/2 (Hz) at intervals of 2/B (sec), said timing extraction circuit comprising:

a detection circuit ~~for~~ detecting the absence of an output of phase comparison information from said phase comparator circuit by receiving a data signal of a prescribed pattern; and

a control circuit ~~for~~ controlling, upon detecting said absence, the phase of said clock signal in order to maintain synchronization.

2. (ORIGINAL) A circuit as claimed in claim 1, wherein said control circuit controls the phase of said clock signal by inverting said clock signal.

3. (CURRENTLY AMENDED) A circuit as claimed in claim 1, wherein said control circuit controls the phase of said clock signal by controlling ~~a VCO~~a voltage controlled oscillator (VCO).

4. (CURRENTLY AMENDED) A timing extraction circuit which uses ~~a PLL~~a phase locked loop (PLL) circuit containing a phase comparator circuit for performing a phase comparison between a data signal of bit rate B (bits/s) and a clock signal of B/2 (Hz) at intervals of 2/B (sec), wherein said phase comparator circuit comprises two phase comparator circuits which respectively accept phases differing by one cycle (1/B sec) of said data signal to perform phase comparisons for all data signals.

5. (CURRENTLY AMENDED) ~~A duty cycle deviation handling circuit for use in an optical receiver~~A discrimination circuit for a data signal having duty cycle deviation for use in an optical receiver, comprising:

~~a PLL~~phase locked loop (PLL) circuit containing a phase comparator circuit for performing a phase comparison between a data signal of bit rate B (bits/s) and a clock signal of B/2 (Hz) at intervals of 2/B (sec);

a duty cycle evaluation circuit for evaluating a duty cycle between input data before and after a point at which said PLL circuit is locked; and

a control circuit for controlling, based on a result of said evaluation, a data discrimination phase before and after the point at which said PLL circuit is locked.

6. (CURRENTLY AMENDED) A circuit as claimed in claim 5, wherein:

said control circuit includes an initial phase setting circuit in which duty cycle information representing an initial phase adjustment is set~~,~~; and

said initial phase setting circuit compares said duty cycle information representing said initial phase adjustment with an output of said duty cycle evaluation circuit and, when locked in phase in the same condition as said duty cycle information representing said initial phase adjustment, said locked condition is maintained, but when locked in phase in a condition different from said duty cycle information representing said initial phase adjustment, a clock output of a voltage-controlled oscillator in said PLL circuit is inverted.

7. (CURRENTLY AMENDED) A circuit as claimed in claim 5, wherein:

said PLL circuit discriminates said input data every other bit by using said clock signal whose frequency is equal to one half the data transmission rate and an inverted version of said clock signal, and achieves a phase lock in accordance with a result obtained by exclusive-ORing the data discriminated by a clock signal delayed in phase by one half cycle of said data signal with the data discriminated by said half-frequency clock signal and the data discriminated by the inverted version of said half-frequency clock signal, respectively, and by comparing average values of said respective exclusive-OR sums,

said duty cycle evaluation circuit evaluates said duty cycle to determine whether said duty cycle changes from "narrow" to "wide" or from "wide" to "narrow" between said input data before and after the point at which said PLL circuit is locked, said evaluation being made based on a result obtained by exclusive-ORing the data discriminated by an inverted version of said

clock signal delayed in phase by one half cycle of said data signal with the data discriminated by said half-frequency clock signal and the inverted version of said half-frequency clock signal, respectively, and by comparing average values of said respective exclusive-OR sums, and

said control circuit, based on the result of said evaluation, controls the phase of said clock signal delayed in phase by one half cycle of said data signal and the phase of the inverted version of said clock signal respectively in opposite directions.

8. (ORIGINAL) A circuit as claimed in claim 7, wherein the discrimination phases of said clock signal and the inverted version thereof for discriminating said data signal are adjusted independently of each other by adjusting the phase of said clock signal independently of the phase of said clock signal delayed in phase by one half cycle of said data signal.